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REMARKS: **Serial No. 10/655,321, filed 09/04/2003.**
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CLIENT/MATTER NO. 200301955-2 (1662-37901)

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PATENT APPLICATION
ATTORNEY DOCKET NO. 200301955-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Richard B. WATSON, Jr., et al. **Confirmation No.:** 5852

Application No.: 10/655,321 **Examiner:** Manuel L. Barbee

Filing Date: 09/04/2003 **Group Art Unit:** 2857

Title: CLOCK SKEW MEASUREMENT CIRCUIT ON A MICROPROCESSOR DIE

Mail Stop Appeal Brief-Patents
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PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

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Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 01/28/2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( ) one month $120.00
( ) two months $450.00
( ) three months $1020.00
( ) four months $1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

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Number of pages: 28

Typed Name: Colleen F. Brown

Signature: Colleen F. Brown

Respectfully submitted,

Richard B. WATSON, Jr., et al.

By [signature]

Mark E. Scott

Attorney/Agent for Applicant(s)
Reg. No. 43,100

Date: 03/24/2005

Telephone No.: (713) 238-8000

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PATENT APPLICATION

ATTORNEY DOCKET NO. 200301955-2

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UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Richard B. WATSON, Jr., et al.

Confirmation No.: 5852

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Examiner: Manuel L. Barbee

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( )	four months	$1590.00

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Number of pages: 28

Typed Name: Colleen F. Brown
Signature: Colleen F. Brown

Respectfully submitted,
Richard B. WATSON, Jr., et al.

By [signature]

Mark E. Scott
Attorney/Agent for Applicant(s)
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Date: 03/24/2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Richard B. Watson, Jr., et al.	§	Confirmation No.:	5852
Serial No.:	10/655,321	§	Group Art Unit:	2857
Filed:	09/04/2003	§	Examiner:	Manuel L. Barbee
For:	Clock Skew Measurement Circuit On A Microprocessor Die	§	Docket No.:	200301955-2

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: March 24, 2005

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed via facsimile on January 28, 2005.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas, through its merger with Compaq Computer Corporation (CCC) which owned Compaq Information Technologies Group, L.P. (CITG). The assignment from the inventors Watson, Mendoza and Bertucci to CITG was recorded on December 26, 2001, at Reel/Frame 012448/0627 and the assignment from inventor Welch to CITG was recorded on July 31, 2002, at Reel/Frame 013137/0061. The Change of Name document was recorded on May 12, 2004, at Reel/Frame 014628/0103.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

Appl. No. 10/655,321
Appeal Brief dated March 24, 2005
Reply to final Office action of November 22, 2004

III. STATUS OF THE CLAIMS

Originally filed claims: 1-61.

Claim cancellations by Preliminary Amendment:

4, 7-16, 18, 21-22, 25-26, 29-31, 25-48, 42-43, 46-48, 51-52 and 54-61 (in favor of those same claims in the parent case).

Claim cancellations during prosecution of the current case:

1-3, 5-6, 17, 39-41, 44 and 53.

Added claims: 62-66.

Presently pending claims: 19-20, 23-24, 27-28, 32-34, 45, 49-50 and 62-66.

Presently allowed claims: 33, 34 and 62.

Presently objected-to claims (allowable if rewritten in independent form):

64.

Presently appealed claims: 19-20, 23-24, 27-28, 32, 45, 49-50 and 63-66.

IV. STATUS OF THE AMENDMENTS

No claims were amended after the final Office action dated November 22, 2004.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The various embodiments of the invention are directed to clock skew measurement on a microprocessor die.[1] At least some of the illustrative embodiments are a method comprising generating on the microprocessor die[2] a first and second reference clock signals having the same frequency but differing in phase relationship[3], defining a time window between features of the first and second reference clock signals[4], comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window[5], adjusting the time window[6], and repeating the comparing and adjusting to determine the uncertainty window.[7]

Other illustrative embodiments may be a system comprising a measurement circuit[8] on the die of the microprocessor[9] and an external measurement system[10] coupled the measurement circuit by way of a scan chain of the microprocessor.[11] The external measurement system executes software that controls the measurement circuit through the scan chain, and adjusts a phase relationship of a plurality reference clock signals having varying phase[12] (the plurality of reference clock signals define a plurality of time windows between

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[1] Specification Title.

[2] Specification Paragraph [0043], lines 2-8 (of the paragraph). Hereinafter, citation to Specification Paragraph and line numbers takes the form ([paragraph], lines [lines spanned]), *e.g.*, for this citation ([0043], lines 2-8).

[3] ([0049], lines 1-3).

[4] ([0049], lines 4-5).

[5] ([0051], lines 3-5).

[6] ([0057], lines 9-12).

[7] ([0061], lines 9-11).

[8] ([0044], lines 1-2; Figure 3).

[9] ([0043], lines 6-8).

[10] ([0057], lines 2-4).

[11] ([0057], lines 8-9).

[12] ([0057], lines 7-12).

corresponding features).[13] The measurement circuit compares the target clock signal to the plurality of time windows[14] to determine the uncertainty window of the target clock signal.[15]

Other illustrative embodiments are a method comprising generating a first and second calibration signal (each calibration signal having the same frequency, but differing in phase relationship by a known period of time)[16], phase locking an output signal of a programmable delay chain to the first calibration signal[17], noting a number of programmable taps required to phase lock to the first calibration signal[18], phase locking the output signal of the programmable delay chain to the second calibration signal[19], noting the number of programmable taps required to phase lock to the second calibration signal[20], attributing the difference in the number of taps to lock to the first and second calibration signal to the known period of time[21], and thereby attributing to each tap a portion of the known period of time.[22]

Yet other illustrative embodiments are a method comprising generating on a microprocessor die a first, second, third and fourth reference clock signals having the same frequency but differing in phase relationship[23], defining a first time bin between respective features of the first and second reference clock signals, defining a second time bin between respective features of the second and third reference clock signals, and defining a third time bin between respective

[13] ([0049], lines 3-5).
[14] ([0051], lines 2-5).
[15] ([0061], lines 9-11).
[16] ([0071], lines 10-13).
[17] ([0072], lines 2-5; [0077], lines 9-10).
[18] ([0078], lines 1-2).
[19] ([0072], lines 2-5; [0079], lines 1-3).
[20] ([0079], lines 7-9).
[21] ([0079], lines 9-10).
[22] ([0080], lines 6-9).
[23] ([0049], lines 1-3).

features of the third and fourth reference clock signals[24], comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine in which bin the target clock signal makes it state transitions[25], adjusting the phase relationship of at least one of the reference clock signals (and thereby adjusting the time width of at least one time bin)[26], and repeating the adjusting and the comparing until the uncertainty window is determined.[27]

Yet still other illustrative embodiments are a method comprising generating on a microprocessor die a first and second reference clock signals having the same frequency but differing in phase relationship[28], defining a time window between features of the first and second reference clock signals[29], comparing on the microprocessor die a plurality of cycles of a target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window[30], adjusting the phase of only one of the first and second reference clock signals to adjust the time window[31], and repeating the comparing and adjusting to determine an uncertainty window within which the target clock makes state transitions.[32]

Further illustrative embodiments may be a method comprising comparing within an electronic device a plurality of cycles of a target clock signal to a first and second reference clock signals to determine whether the target clock signal makes state transitions within a time window between features of the reference

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[24] ([0049], lines 4-5).

[25] ([0051], lines 3-5).

[26] ([0057], lines 9-12).

[27] ([0061], lines 9-11).

[28] ([0049], lines 1-3).

[29] ([0049], lines 4-5).

[30] ([0043], lines 2-8; [0051], lines 3-5).

[31] ([0059], lines 1through [0060], line 7 (note how each reference clock is independently adjustable)).

[32] ([0061], lines 9-11).

clock signals[33], adjusting the phase of the first and second reference clock signals[34] (wherein phases of the plurality of reference clock signals are independently controlled)[35], and repeating the comparing and independently adjusting to determine an uncertainty window within which the target clock on the electronic device makes state transitions.[36]

Some illustrative embodiments are a system comprising a clock domain region of an electronic device[37], and a jitter measurement circuit.[38] The jitter measurement circuit comprises a plurality of delay units[39] creating a plurality of reference clock signals having the same frequency but differing in phase relationship[40] (wherein the phase delay of each reference clock signal is independently controlled)[41], and a measurement unit coupled to the plurality of reference clock signals and a target clock[42] (wherein the measurement unit compares the target clock to the plurality of reference clock signals to determine an uncertainty window within which the target clock makes state transitions).[43]

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[33] ([0051], lines 3-5; [0049], lines 4-5).

[34] ([0057], lines 9-12).

[35] ([0059], lines 1through [0060], line 7).

[36] ([0061], lines 9-11).

[37] ([0039], lines 3-9; Figure 2).

[38] ([0043], lines 5-6; Figures 2 and 3).

[39] ([0044], lines 6-8; Figures 3 and 6).

[40] ([0049], lines 2-5).

[41]([0059], line 1through [0060], line 7).

[42] ([0044], lines 10-13; Figure 3).

[43] (*Id.*).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 19-20, 23-24, 45, 49-50, 63 and 65 are anticipated by Kelkar (U.S. Pat. No. 5,663,991).

Whether claims 27-28, 32 and 66 are unpatentable over Kelkar in view of Neudeck (U.S. Pat. No. 5,701,335).

VII. ARGUMENT

Before addressing the specifics of the rejections of the Office action dated November 22, 2004, it is helpful to put into context the primary reference, Kelkar. This following discussion is not directed to any particular appealed claim; rather, the shortcomings of the rejections are discussed more fully below.

Kelkar is directed to an integrated circuit chip having built-in self measurement for PLL jitter and phase error.[44] Kelkar's Figure 2, reproduced immediately below, is indicative of a first embodiment of the Kelkar system.

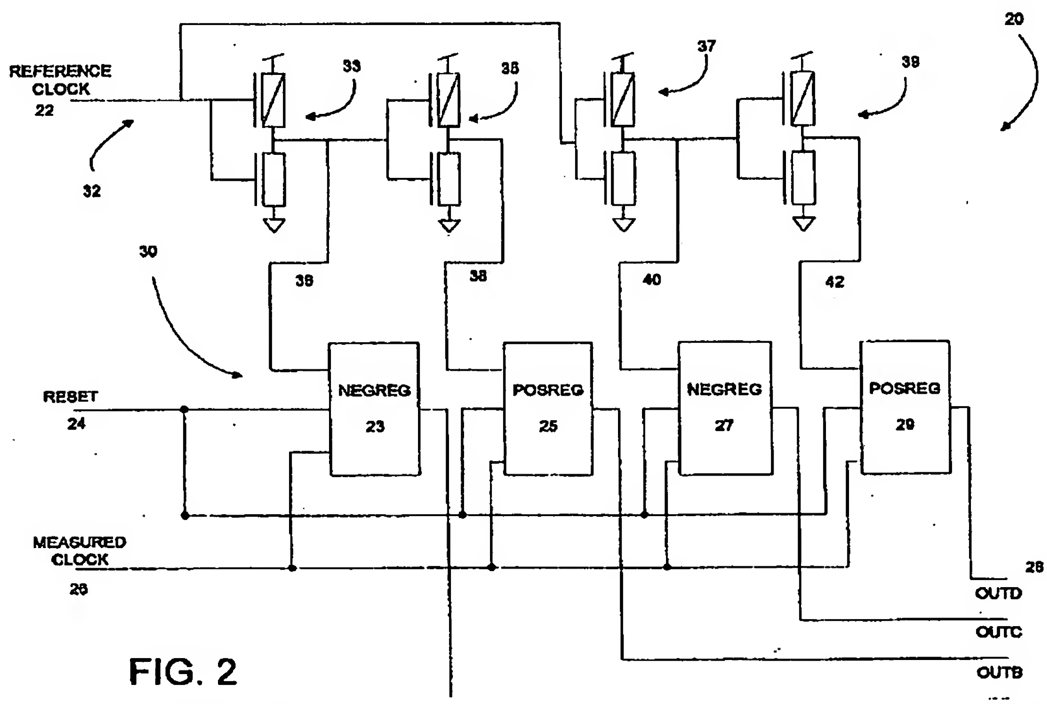

FIG. 2

In particular, Kelkar discusses the four delay line elements 33, 35, 37 and 39 create four delayed clock signals 36, 38, 40 and 42.[45] The measured clock 26 is compared to the delayed clock signals by the latches 23, 25, 27 and 29.[46] However, while Kelkar discusses the delay induced by the four delay line

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[44] Kelkar, Title.

[45] Kelkar, Col. 3, lines 62-67.

[46] Kelkar, Col. 4, lines 11-16.

elements 33, 35, 37 and 39 to be a "predetermined amount of time,"[47] the "predetermined amount of time" of Kelkar's Figure 2 is not controllable after chip-level construction of the constituent transistors.

> Each delay element comprises a transistor pair suitable for causing the reference signal, or the output of a prior delay element, to be delayed by **a predetermined amount of time**. For example, the four delay line elements may provide time delays of 100, 200, 300 and 400 picoseconds respectively. ... (FIGS. 5 and 6 depict an alternate embodiment of a system **for generating calibrated time slices** using delay elements **with controllable delay** and a calibration circuit.)[48]

Thus, for "controllable delay," Kelkar directs the reader to Kelkar's Figures 5 and 6.

Kelkar's Figure 5 discloses "a system 80 for generating calibrated time slices using delay elements with controllable delay... ."[49] However, the "controllable delay" taught by Kelkar **is only to compensate the delay line 83 for influences that change the desired delay**, such as manufacturing inconsistencies, operating temperature and supply voltage swings.

> By using the calibration system, the total delay is automatically adjusted to the desired amount. **Process variations as well as environmental differences in temperature and power supply voltage can be automatically tuned out using this calibration circuit.**[50]

Further, the "controllable delay" of Kelkar is only concerned with keeping a one period time difference between the test clock 84 and the output clock 87 in spite of process variations, difference in temperature and differences in supply voltage.

> Both the test clock 84 and output clock 87 are applied to a phase detector 88 input. The phase detector output controls a charge pump 90 that charges or discharges a loop filter capacitor 86, which provides the delay control signal 85 to the variable delay line 83. **The**

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[47] Kelark, Col. 3, line 67 through Col. 4, line 3.

[48] *Id.* (emphasis added); *see also* Figure 2 which fails to illustrate any mechanism to change the delay through the delay chain.

[49] Kelkar, Col. 5, lines 46-48.

[50] Kelkar, Col. 6, lines 28-32 (emphasis added).

> **feedback loop tries to maintain zero phase shift between the test clock 84 and output clock 87. Thus, the calibration circuit works by forcing the total delay to be equal to one period of the test clock 84.**[51]

Thus, the "controllable delay" of Kelkar is only to **maintain a total delay equal to one period of the test clock.**

A. Claims 19-20, 23-24, 45, 49-50, 63 and 65

Claims 19-20, 23-24, 45, 49-50, 63 and 65 stand rejected as allegedly anticipated by Kelkar. Claim 45 is representative of this grouping of claims. The grouping, however, is for purposes of this appeal only. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the grouping. Rather, the presumption of 35 U.S.C. § 282 shall apply to each claim individually.

Claim 45 specifically recites, "comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine in which bin the target clock signal makes it state transitions; [and] **adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin."** Appellants respectfully submit that Kelkar fails to teach or fairly suggest the limitations of representative claim 45. In particular, Kelkar's adjustment to the delay line 83 is only to ensure that the total delay through the delay line 83 is maintained equal to one period of the test clock, and **therefore the bins ("time slices" in Kelkar terminology) defined remain <u>constant</u> in spite of process variations, difference in temperature and differences in supply voltage.** Thus, Kelkar fails to teach or suggest "adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin." In fact, Kelkar teaches away from adjusting the phase relationship to adjust at least one time bin.

In the Response to Arguments section of the Final Office action dated November 22, 2004, the position is taken that, "Adjustments of the time windows

[51] Kelkar, Col. 5, line 64 – Col. 6, line 6 (emphasis added); Figure 5)

may be triggered by a change in the frequency of the test clock, or by process variations."[52] Addressing the second assertion first, inasmuch as the representative claimed method requires that the reference clock signals are generated on the microprocessor die[53], Appellants fail to see how Kelkar could teach or suggest "adjusting the phase relationship ... and thereby adjusting the time width of at least one time bin" by "process variations"[54] on a microprocessor die that is already constructed. As Appellants read Kelkar, changing the time slices for a particular clock frequency requires a different design of the delay circuits.

With respect to adjusting the time windows by "a change in the frequency of the test clock," Appellants acknowledge that claims are to be given their broadest reasonable interpretation during prosecution; however, Appellants respectfully submit that interpreting the claims of this grouping to cover changing the frequency of the test clock to achieve the claimed adjusting the phase relationship is an unreasonable interpretation. First, if the frequency of Kelkar's reference clock is changed slightly to change the time slice time widths, and Kelkar's measured clock frequency remains the same, then Kelkar cannot measure an uncertainty window. In particular, in this circumstance the relationship between the phase of the reference clock (and therefore the features of the reference clock signals defining the time bins) and the phase of the measured clock in relation to the phases of the reference clocks changes every period, rendering the system unable to meet Appellants' claimed measurement of the uncertainty window. The following illustration, an adaptation of the Appellants' Figures 1A-C and 9, illustrates the fallacy of the assertion.

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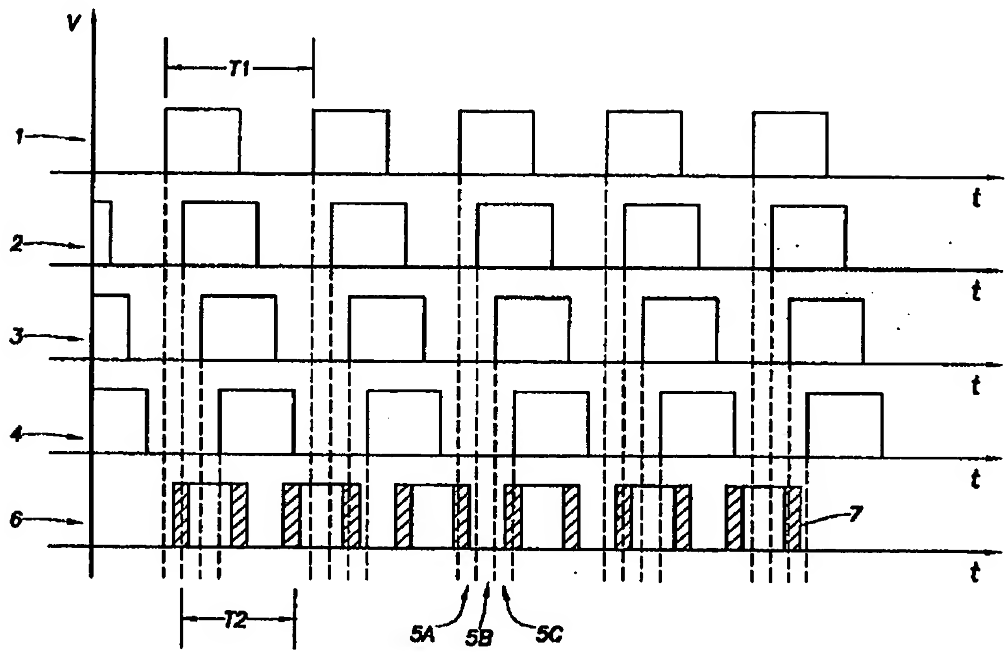
[52] Office action dated November 22, 2004, Page 8, Paragraph 8.

[53] Claim 45, first recited limitation after the preamble.

[54] *E.g.*, variations in transistor speeds across a microprocessor die caused by irregularities in doping and etching during manufacture. ([0006], lines 5-7).



In particular, the above illustration shows four delayed clock signals 1-4, each have a period T1 (*i.e.*, each reference clock having the same frequency), but differing slightly in phase relationship so as to define three time bins each period (*e.g.*, time bins 5A-C). Plotted on the same vertical axis is an illustrative measured clock signal 6 having a period T2 less than T1, and each transition having an uncertainty window, *e.g.*, uncertainty window 7. As can be clearly seen, and even taking into account the uncertainty windows, because of the difference in frequency, the measured clock makes state transitions seemingly randomly across the time bins, thus rendering a Kelkar system modified as suggested by the Examiner incapable of determining the uncertainty window.

Further with regard to the assertion that, "Adjustments of the time windows may be triggered by a change in the frequency of the test clock... ,"[55] if the interpretation is that both the Kelkar's reference clock and the measured clock

[55] Office action dated November 22, 2004, Page 8, Paragraph 8.

frequency change, Appellants respectfully traverse the assertion that an uncertainly window for a measured clock of a particular frequency can be determined by reference to a measured clock of a second, different frequency.

Appellants respectfully submit that Kelkar fails to teach or fairly suggest the limitations of representative claim 45, and thus the rejections of claims 19-20, 23-24, 45, 49-50, 63 and 65 in the Office action dated November 22, 2004 should be overturned.

B. Claims 27-28, 32 and 66

Claims 27-28, 32 and 66 stand rejected as allegedly obvious over Kelkar and Neudeck. Claim 27 is representative of this grouping of claims. The grouping, however, is for purposes of this appeal only. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the grouping. Rather, the presumption of 35 U.S.C. § 282 shall apply to each claim individually.

Claim 27 specifically recites, "wherein the external measurement system adjusts a phase relationship of a plurality reference clock signals having varying phase, the plurality of reference clock signals define a plurality of time windows between corresponding features; and wherein the measurement circuit compares the target clock signal to the plurality of time windows to determine the uncertainty window of the target clock signal." Appellants respectfully submit that Kelkar and Neudeck fail to teach or fairly suggest the limitations of representative claim 27. In particular, Kelkar's adjustment to the delay line 83 is only to ensure that the total delay through the delay line 83 is maintained equal to one period of the test clock, and **therefore the bins ("time slices" in Kelkar terminology) defined remain <u>constant</u> in spite of process variations, difference in temperature and differences in supply voltage**. Thus, even if the teachings of Neudeck are precisely as suggested (which Appellants do not admit), Kelkar and Neudeck fail to teach or suggest a system that "adjusts a phase relationship of a plurality reference clock signals having varying phase;... and wherein the measurement circuit compares the target clock signal to the plurality of time windows to determine the uncertainty window of the target clock signal." In fact,

Kelkar teaches keeping the phase relationship constant with the "controllable delay," and therefore teaches away from adjusting the phase relationship. For at least this reason alone, the rejection regarding this grouping of claims should be overturned.

Representative claim 27 further requires, "an external measurement system coupled the measurement circuit by way of a scan chain of the microprocessor, and wherein the external measurement system executes software that controls the measurement circuit through the scan chain; ... wherein the external measurement system adjusts a phase relationship of a plurality reference clock signals having varying phase." In Kelkar's system, the control of the delay line 83 is only **to maintain a total delay equal to one period of the test clock**. No external measurement system that controls the delay line 83 is taught, suggested or even implied. Thus, even if the teachings of Neudeck's scan chain are precisely as suggested (which Appellants do not admit), Kelkar and Neudeck still fail to teach "an external measurement system coupled the measurement circuit by way of a scan chain of the microprocessor, and wherein the external measurement system executes software that controls the measurement circuit through the scan chain; ... **wherein the external measurement system adjusts a phase relationship of a plurality reference clock signals having varying phase.**" For this additional reason, the rejection regarding this grouping of claims should be overturned.

Appellants respectfully submit that Kelkar and Neudeck fail to teach or fairly suggest the limitations of representative claim 27, and thus the rejections of claims 27-28, 32 and 66 in the Office action dated November 22, 2004 should be overturned.

VIII. CONCLUSION

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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Intellectual Property Administration
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IX. CLAIMS APPENDIX

1.-18. (Canceled).

19. (Previously presented) A method of measuring an uncertainty window within which a target clock signal on a microprocessor die makes state transitions, the method comprising:

generating on the microprocessor die a first and second reference clock signals having the same frequency but differing in phase relationship;

defining a time window between features of the first and second reference clock signals;

comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window;

adjusting the time window; and

repeating the comparing and adjusting to determine the uncertainty window.

20. (Original) The method of measuring an uncertainty window as defined in claim 19 wherein generating the first and second reference clock signal on the microprocessor die further comprises:

coupling a core clock signal to a first adjustable delay chain;

delaying the core clock by a first length of time with the first adjustable delay chain to create the first reference clock signal;

coupling the core clock signal to a second adjustable delay chain; and

delaying the core clock by a length of time greater than the first length of time with the second adjustable delay chain to create the second reference clock signal.

21.-22. (Canceled).

23. (Original) The method of measuring an uncertainty window as defined in claim 19 wherein defining the time window further comprises defining the time window between corresponding low voltage to high voltage state transitions of the first and second reference clock signals.

24. (Original) The method of measuring an uncertainty window as defined in claim 19 wherein adjusting the time window further comprises adjusting the phase relationship of the first and second reference clock signals.

25.-26. (Canceled).

27. (Previously presented) A system for measuring an uncertainty window of a target clock signal of a microprocessor, the system comprising:

a measurement circuit on the die of the microprocessor;

an external measurement system coupled the measurement circuit by way of a scan chain of the microprocessor, and wherein the external measurement system executes software that controls the measurement circuit through the scan chain;

wherein the external measurement system adjusts a phase relationship of a plurality reference clock signals having varying phase, the plurality of reference clock signals define a plurality of time windows between corresponding features; and

wherein the measurement circuit compares the target clock signal to the plurality of time windows to determine the uncertainty window of the target clock signal.

28. (Original) The system for measuring the uncertainty window as defined in claim 27 wherein the measurement circuit further comprises:

a plurality of delay units each coupled to a host clock and creating the plurality of reference clock signals by selectively phase delaying the host clock signal by each of the delay units; and

a measurement unit coupled to the plurality of reference clock signals and the target clock signal, and wherein the measurement unit compares the plurality of reference clock signals to the target clock signal to determine the uncertainty window.

29.-31. (Canceled).

32. (Previously presented) The system for measuring the uncertainty window as defined in claim 27 wherein the external measurement system further comprises a microcontroller adapted to execute software algorithms coupled to the measurement circuit by way of the scan chain.

33. (Previously presented) In a system for measuring on the die of the electronic device an uncertainty window within which a target clock signal may make a state transition, a method of calibrating a measurement circuit comprising:

generating a first and second calibration signal, each calibration signal having the same frequency, but differing in phase relationship by a known period of time;

phase locking an output signal of a programmable delay chain to the first calibration signal;

noting a number of programmable taps required to phase lock to the first calibration signal;

phase locking the output signal of the programmable delay chain to the second calibration signal;

noting the number of programmable taps required to phase lock to the second calibration signal;

attributing the difference in the number of taps to lock to the first and second calibration signal to the known period of time; and thereby

attributing to each tap a portion of the known period of time.

34. (Original) The method of calibrating a measurement circuit as defined in claim 33 wherein generating the first and second calibration signal further comprises:

applying a host clock signal to a first delay element having known propagation delay to create the first calibration signal; and

applying the first calibration signal to a second delay element having known propagation delay to create the second calibration signal.

35.-44. (Canceled).

45. (Previously presented) A method for determining an uncertainty window within which a target clock signal of an electronic device makes state transitions, the method comprising:

generating on a microprocessor die a first, second, third and fourth reference clock signals having the same frequency but differing in phase relationship;

defining a first time bin between respective features of the first and second reference clock signals, defining a second time bin between respective features of the second and third reference clock signals, and defining a third time bin between respective features of the third and fourth reference clock signals;

comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine in which bin the target clock signal makes it state transitions;

adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin; and

repeating the adjusting and the comparing until the uncertainty window is determined.

46.-48. (Canceled).

49. (Original) The method of measuring an uncertainty window as defined in claim 45 wherein defining the time window further comprises defining the time window between corresponding low voltage to high voltage state transitions of the first and second reference clock signals, second and third reference clock signals, and the third and fourth reference clock signals.

50. (Previously presented) The method of measuring an uncertainty window as defined in claim 45 wherein adjusting the time bins further comprises adjusting the phase relationship of at least one of the first, second, third or fourth reference clock signals.

51.-61. (Canceled).

62. (Previously presented) A method comprising:
generating on a microprocessor die a first and second reference clock signals having the same frequency but differing in phase relationship;
defining a time window between features of the first and second reference clock signals;
comparing on the microprocessor die a plurality of cycles of a target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window;
adjusting the phase of only one of the first and second reference clock signals to adjust the time window; and
repeating the comparing and adjusting to determine an uncertainty window within which the target clock makes state transitions.

63. (Previously presented) A method comprising:
comparing within an electronic device a plurality of cycles of a target clock signal to a first and second reference clock signals to determine

whether the target clock signal makes state transitions within a time window between features of the reference clock signals;

adjusting the phase of the first and second reference clock signals, wherein phases of the plurality of reference clock signals are independently controlled; and

repeating the comparing and independently adjusting to determine an uncertainty window within which the target clock on the electronic device makes state transitions.

64. (Previously presented) The method as defined in claim 63 further comprising:

generating the first and second reference clock signals within the electronic device;

phase delaying the second reference clock signal more than the first reference clock signal; and

defining the time window between features of the first and second reference clock signals.

65. (Previously presented) A system comprising

a clock domain region of an electronic device; and

a jitter measurement circuit comprising

a plurality of delay units creating a plurality of reference clock signals having the same frequency but differing in phase relationship, wherein the phase delay of each reference clock signal is independently controlled; and

a measurement unit coupled to the plurality of reference clock signals and a target clock, wherein the measurement unit compares the target clock to the plurality of reference clock signals to determine an uncertainty window within which the target clock makes state transitions.

66. (Previously presented) The system as defined in claim 65 wherein each of the plurality of delay units couples to a scan chain, and wherein an external device controls the phase delay created by each delay unit by communicating with each delay unit over the scan chain.